WHAT IS CLAIMED IS:

1. A method for synchronizing the data interchange in a semiconductor substrate integrated electronic circuit comprising a transmitter block and a receiver block connected through a communication network, comprising:

generating a data signal having a transmission period on a first line that from said transmitter block must be received by the receiver block;

generating on a second line a congestion signal from the receiver block to the transmitter block when a congestion event of the receiver block occurs in order to interrupt the transmission of said data signal; and

generating on a third line a synchro signal starting from said transmitter block, this synchro signal indicating to the receiver block that the data signal comprises a new datum, and in that the congestion signal interrupts also the transmission of said synchro signal when a congestion event of the receiver block occurs.

2. The method for synchronizing the data interchange according to claim 1, wherein said synchro signal is delayed with respect to the data signal.

3. The method for synchronizing the data interchange according to claim 2, wherein said synchro signal is delayed by half transmission period with respect to the data signal.

4. The method for synchronizing the data interchange according to claim 1, further including reading, by the receiver block, of the data signal with a different sampling period from the transmission period of the transmitter block.

5. The method for synchronizing the data interchange according to claim 1, further including reading, by the receiver block, of the data signal with a lower sampling period than the transmission period of the transmitter block.

6. The method for synchronizing the data interchange according to claim 1, wherein said first, second and third lines are split in corresponding stages, each stage being separated through a corresponding repeater, the repeaters of the first and third lines being of the tristate type and being driven by the repeater of the second line when a congestion event occurs at the receiver block so that the data signal and the synchro signal are stored in the stages of the first and third lines.

7. The method for synchronizing the data interchange according to claim 6, wherein said stages have an elementary delay which must be lower than half the transmission period.

8. The method for synchronizing the data interchange according to claim 1, further including generating, on a couple of further lines, a couple of unidirectional signals indicating the transmission direction between said transmitter block and said receiver block, a negotiation

to define the transmission direction being controlled by a further transmission request signal driven by the receiver block.

9. An integrated electronic circuit being integrated on a semiconductor substrate comprising a transmitter block and a receiver block connected through a communication network, said communication network comprising a first line for a data signal, a second line for a congestion signal, and a third line for a synchro signal, wherein said first, second and third lines are split in corresponding stages, each stage being separated through a corresponding repeater, the repeaters of the first and third lines being of the tristate type and being driven by the repeater of the second line when a congestion event of the receiver block occurs so that the data signal and the synchro signal are stored in the stages of the first and second lines.

10. The integrated electronic circuit of claim 9 wherein said signal line comprises a couple of further lines for a couple of unidirectional signals indicating the transmission direction between said transmitter block and said receiver block, a negotiation to define the transmission direction being controlled by a further transmission request signal driven by the receiver block.

11. An architecture for manufacturing an integrated electronic circuit being integrated on a semiconductor substrate comprising a transmitter block and a receiver block connected through a communication network, said communication network comprising a plurality of signal lines each split in elementary blocks, each block being separated through a repeater, said elementary blocks being connected to said receiver and transmitter blocks through interface devices equipped with unidirectional signals.

12. The architecture according to claim 11, wherein said signal lines comprise a couple of further lines carrying unidirectional signals indicating the transmission direction between said transmitter block and said receiver block, a negotiation to define the transmission direction being controlled by a further transmission request signal driven by the receiver block.

13. The architecture according to claim 11, wherein each elementary block is realized through a multiplexer 2x2.

14. A communication protocol, comprising:

transmitting along with a data signal a synchronization signal indicating to a receiving entity that the data signal comprises new datum; and

inhibiting transmission of the synchronization signal in response to an indication received from the receiving entity of the existence of a congestion condition at the receiving entity.

15. The protocol as in claim 14, wherein the data signal is communicated on a first communication line and the synchronization signal is communicated on a second communication line.

16. The protocol as in claim 15, wherein the indication of the existence of a congestion condition at the receiving entity is received over a third communication line.

17. The protocol as in claim 14 further including inhibiting transmission of the data signal in response to the indication received from the receiving entity of the existence of a congestion condition at the receiving entity.

18. The protocol as in claim 14 wherein transmitting comprises sending the synchronization signal delayed with respect to the data signal.

19. A communication system, comprising:

a first communication block;

a second communication block;

a communication network interconnecting the first and second communication blocks, the communication network comprising:

a first communication line for carrying a data signal;

a second communication line for carrying a congestion signal; and

a third communication line for carrying a synchronization signal, wherein the synchronization signal is active whenever the data signal on the first communication line is new datum and inactive whenever the congestion signal on the second communication line is active.

20. The system of claim 19, wherein the first, second and third communication lines are each split into corresponding stages, further comprising:

a repeater device separating consecutive ones of the stages.

21. The system of claim 20, wherein the repeater devices for the first and third communication lines are of a tristate type wherein the repeater devices of the second communication line drive the tristate operation of the repeater devices for the first and second communication lines in response to the congestion signal being active so that the data signal and the synchronization signal are stored in stages of the first and second communication lines.

22. The system of claim 19, wherein the first, second and third communication lines are bi-directional, further including:

a transmit signal line; and

a receive signal line;

wherein the transmit and receive signal lines interconnect the first and second communication blocks, and control signals thereon specify which of the first and second communication blocks is a transmitter of the data signal and which of the first and second communication blocks is a receiver of the data signal.

23. The system of claim 22, further including a request signal line that interconnects the first and second communication blocks, and a control signal thereon used to negotiate which of the first and second communication blocks is to be transmitter/receiver.

24. The system of claim 19, wherein transmission of the data signal on the first communication line is inhibited whenever the congestion signal on the second communication line is active.

25. The system of claim 19, wherein the active synchronization signal is delayed with respect to transmission of the data signal on the first communication line.